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***ECL34XX Digital Logic and Computer Organization Lab***

**L-T-P-Cr: 0-0-3-1**

**Pre-requisites:** Elements of Electronics Engineering

**Objectives/Overview:**

* This lab course indented to make students familiar with all varieties of Digital Circuits (both combinational & sequential circuits) & timing circuits, their design & applications along with Analog to Digital & Digital to Analog conversion.

**Course Outcomes:**

At the end of the course, a student should:

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| **Sl. No.** | **Outcome** | **Mapping to POs** |
|  | Learn the basic methods for the design of digital circuits and provide the fundamental concepts used in the design of digital systems. | PO1, PO3 |
|  | Understand and design combinational circuits such as logic gates, adder, subtractor, parity generator and checker, Decoder, Multiplexer and De-multiplexer. | PO1, PO5 |
|  | Understand and design sequential circuits such as flip-flops, shift registers, counters. | PO3, PO1 |
|  | Analyze and design various analog to digital & digital to analog converters  | PO3, PO5 |
|  | Design digital circuits using MultiSIM | PO1, PO3 |

**List of Experiments:**

1. Universal Gates (i) Identification and verification of NAND gate (IC #7400) and NOR gate (IC #7402). (ii) Construction and Verification of all other gate (AND, OR, NOT, XOR) USING a) Only NAND gate b) Only NOR gate Introduction to SQL: Basic DML, DDL, DTL commands.
2. Code Convertor & Parity Generator and checker. (i) Identification & verification of NOT (7404), AND (7408) OR (7432) & XOR (7486) gates. (ii) Design, construction and verification of 3-bit Binary to Gray convertor and 3-bit Grey to Binary convertor circuit. (iii) Design, construction and verification of 3-bit odd/even Parity Generator and 4-bit odd/even parity checker circuit. Table handling: Alter, Drop Table, Insert Records.
3. Adder, Subtractor & Magnitude comparator circuits. (i) Design, construction and verification of Half Adder and Half Subtractor circuit. (ii) Design, construction and verification of Full Adder and Full Subtractor circuit. (iii) Design, construction and verification of 1-bit and 4-bit Magnitude comparator. (iv) BCD Adder/Subtractor.
4. Decoder, MUX & DMUX (i) Construction and verification of BCD to 7-segment decoder using IC # 7447 (ii) Verification of 4:1 MUX, 8:1 MUX & 16:1 MUX. (iii) Verification of 1:4 DMUX, 1:8 DMUX (iv) Cascading of MUIX and Cascading of Decoders. Join Concept: Simple, Equi, Self, Outer.
5. Latches and Flip Flops (i)Construction and Verification of a Latch circuit using NAND/NOR gates. (ii) Construction and Verification of S-R Flip Flop using above Latch circuits. (iii) Verification of J-K Flip Flop using IC # 7476 (Dual J-KFF) (iv) Construction and Verification of D-Flip Flop and T-Flip Flop using J-K FF (IC #7476). (v) Construction and Verification of Master Slave J-K Flip Flop. Synonym Introduction: Creating object type, Aliasing.
6. Mini project allocation
7. Shift Registers (i) Verification of D-FF using IC # 7474 (Dual D- FF). (ii) Construction and verification of a 2-bit Shift Right Register using IC # 7474 (iii) Construction and verification of a 2-bit Shift Left Register using IC # 7474 (iv) Verification of SISO, SIPO, PISO & PIPO Shift Registers. Introduction to View: create, update, drop.
8. Synchronous & Asynchronous Counters (i) Construction and verification of 2-bit Ripple counter using J-K FF. (ii) Construction and verification of Mod-3 up and Mod-3 down synchronous counter. (iii) Construction and verification of 2-bit Ring counter using J-K FF. (iv) Construction and verification of 2-bit twisted Ring (Johnson) counter using J-K FF. Introduction to PL/SQL: Advantages, Support, Execution.
9. Design and construction of a 4 bit sequence geneator.

Course instructor can add experiments to the above list and/or modify some of the experiments in the above list depending upon course contents covered and examples used in the corresponding theoretical course.